



# International Parallel Machines

## IPM Series

### Overview

Maple Systems' OIT Family Operator Interface Terminals (Maple OITs) communicate with International Parallel Machines (IPM) controllers using the Modbus Network-Generic communications protocol. The Maple OIT is the master in a point-to-point single master, single slave format. The Remote Terminal Unit (RTU) transmission mode is implemented, requiring the IP3416 Controller to be set to this mode.

**NOTE:** Since the International Parallel Machines controllers do not support individual bit access of internal registers, the OIT3100 and OIT4100 Series MicroOITs are the only supported Maple OITs.

Compatible Controllers	
Family	Model
IPM	IP3416, IP3416DL, IP3415RM, IP3416A

### Communications Cable

The Maple OIT should be connected to the RS-485 port of the IPM Series Controller. A list of communications cables offered by Maple Systems as well as cable assembly instructions to assist you in assembling your own communications cable are available on our website at [www.maple-systems.com/cables.htm](http://www.maple-systems.com/cables.htm).

**WARNING:** If your communications cable is not wired exactly as shown in our cable assembly instructions, damage to the Maple OIT or loss of communications can result.

### Controller Settings

DIP Switch #2 must be set to the off position to put the Controller into slave mode (the DIP switches are located at the lower left hand corner of the Controller).

# Accessible Controller Memory

## Register Memory

The following table lists the Controller's register memory ranges that Maple's OITs are able to access. Please note that your Controller's memory range may be *smaller* or *larger* than that supported by Maple's OITs. The following register memory is displayable in 16-bit or 32-bit formats on the Maple OIT.

Register Address	Register Description	Access
T0 to T31 (400001 to 400032, sub0)	Timer Current, 16 Bit Format, 15 Bit Value	Read
C0 to C31 (400033 to 400064, sub0)	Counter Current, 16 Bit Format, 15 Bit Value	Read
D0 to D47 (400065 to 400096, sub0)	Data Register, 16 Bit Format, 16 Bit Value	Read/Write
A24 to A31 (300121 to 300128, sub0)	Analog Input, 16 Bit Format, 16 Bit Value	Read

## Discrete Memory

The following table lists the Controller's discrete memory ranges that Maple's OITs are able to access. Please note that your Controller's memory range may be *smaller* or *larger* than that supported by Maple's OITs.

The R bit-registers are accessed in the protocol as 16-bit words. Writing a bit to a register that is not accessed in a bit-wise fashion requires reading the entire register, changing the bit, then writing back the entire register. Special considerations are required so that the R registers are not changed by the controller during the reading and writing cycle of these registers. One way would be to use the R registers as separate 16-bit banks, with each bank allowed write access by either, but not both, the OIT or the controller.

The following discrete memory is displayable in single-bit or bank formats on the Maple OIT.

Bit Address	Bit Description	Access
X0 to X47 (000001 to 000033)	Input Coil, 1 Bit Format	Read
Y0 to Y15 (100001 to 100016)	Output Coil, 1 Bit Format	Read/Write
T0 to T31 (400001 to 400032, sub15)	Timer Coil, 16 Bit Format, 1 Bit Value	Read
C0 to C31 (400033 to 400064, sub15)	Counter Coil, 16 Bit Format, 1 Bit Value	Read
R0 to R255 (400097sub0 to 400112sub15)	Relay Register, 16 Bit Format, 1 Bit Value	Read/Write

## Important Memory Considerations

If your controller's memory range is smaller than the range supported by Maple's OITs, it is possible to configure the Maple OIT to monitor a memory address which does not exist. Since this can cause unpredictable results, when you configure the Maple OIT please ensure that all selected memory addresses are valid for the controller model.

Do not configure the Maple OIT to write to any memory address which should only be written to by the controller.

**On using Bank 8 or Bank 16 formats**

When using these formats, each controller coil (bit) is individually displayed in terms of 1 and 0, with the lowest addressed coil displayed in the left-most position in the field. Therefore, if using coils 00001-00016, then 00016 is the least significant bit displayed in the right-most position and 00001 is the most significant bit displayed in the left-most position. The address used must start on a byte boundary when using these formats, which can be determined if the first coil's address, minus 1 and then divided by 16, leaves no remainder.

## OITware-200 Settings

The following table lists the communications settings that must be configured in OITware-200.

Please note:

- The Setting column lists OITware-200's recommended setting; OITware-200's default and your controller's default may be different.
- The Options column lists OITware-200's options; your controller may not support every option.

Name	Setting	Options	Important Notes
Baud Rate	9600	19200, 9600, 4800, 2400, 1200, 600, 300	Must match the Controller's settings. Use the fastest baud rate supported by both.
Parity	None	Even, Odd, None, Mark, Space	Must match the Controller's settings.
Data Bits	8	7, 8	Must match the Controller's settings.
Stop Bits	1	1, 2	Must match the Controller's settings.
Status Coils	Disabaled	No options	Not supported due to the lack of bit addressing of internal registers.
Address, Source Address	N/A		
Destination Address	1	1 to 247	Must match the Controller's address.
Password	N/A		
Message Request Register	400095 (D30)	400065 to 400096 Sub=0 (D0 to D31)	Must be within the Controller's supported memory range.
Current Message Register (optional)	400096 (D30)	400065 to 400096 Sub=0 (D0 to D31)	Must be within the Controller's supported memory range.
Function Key Coils (optional)	Disabled		Use the Screen Dependent Function Key Coils instead.
Screen Dependent Function Key Coils (optional)	400095 (D30)	400097 to 400112 Sub=0 (R0 to R255)	Must be within the Controller's supported memory range. Applies to OITs with Screen Dependent Function Keys.
Control Key Coils (optional)	OIT Action	No options	Not supported due to the lack of bit addressing of internal registers.