



Siemens

S7-200 Series

Overview

Maple Systems’ MAP Family & OIT Family Operator Interface Terminals (Maple OITs) communicate with Siemens S7-200 Programmable Logic Controllers (PLCs) using the Profibus PPI communications protocol. The Maple OIT is the master in a point-to-point single master, single slave format.

| Compatible PLCs | |
|-----------------|--|
| Family | Model |
| S7-200 | S7-212, S7-214, S7-215, S7-216 S7-221, S7-222, S7-224, S7-226 |

Communications Cable

The Maple OIT should be connected to the RS-485 network connection, but only supports a single OIT connected to a single PLC. A list of communications cables offered by Maple Systems as well as cable assembly instructions to assist you in assembling your own communications cable are available on our website at www.maple-systems.com/cables.htm.

WARNING: If your communications cable is not wired exactly as shown in our cable assembly instructions, damage to the Maple OIT or loss of communications can result.

OIT Hardware Settings

The OIT3160, OIT3165, OIT3175, OIT3600, OIT4160, OIT4165 and OIT4175 do not require any hardware configuration.

To configure the OIT3200, OIT3250, OIT4400, OIT4450 and OIT5400 for the S7 protocol, Jumper JP4 MUST be set to position B. This jumper can be located as follows:

1. Remove the back cover from the OIT.
2. Position the OIT so that the communication and power connectors are on the bottom of the OIT when viewed from the back.
3. Jumper JP4 is located just left of the board-mounted buzzer. The buzzer is a black, cylindrical object approximately one inch (25mm) in diameter.

Accessible PLC Memory

Register Memory

The following table lists the PLC's register memory ranges that Maple's OITs are able to access. Please note that your PLC's memory range may be *smaller* or *larger* than that supported by Maple's OITs. The following register memory is displayable in 16-bit or 32-bit formats on the Maple OIT.

| PLC Register Address | PLC Register Description |
|----------------------|-----------------------------------|
| V0 to V5119 | Variable Memory Registers |
| T0 to T255 | Timer Current Values |
| C0 to C255 | Counter Current Values |
| HC0 to HC2 | High Speed Counter Current Values |
| AI0- to AI30 | Analog Input Registers |

Discrete Memory

The following table lists the PLC's discrete memory ranges that Maple's OITs are able to access. Please note that your PLC's memory range may be *smaller* or *larger* than that supported by Maple's OITs. The following discrete memory is displayable in single-bit or bank formats on the Maple OIT.

| PLC Bit Address | PLC Bit Description |
|------------------|----------------------|
| M0.0 to M31.7 | Internal Memory Bits |
| I0.0 to I7.7 | Input Image Coils |
| Q0.0 to Q7.7 | Output Image Coils |
| SM0.0 to SM194.7 | Special Memory Bits |
| S0.0 to S31.7 | Stage Memory |
| V0.0 to V5119.7 | Variable Memory Bits |

Important Memory Considerations

If your PLC's memory range is smaller than the range supported by Maple's OITs, it is possible to configure the Maple OIT to monitor a PLC memory address which does not exist. Since this can cause unpredictable results, when you configure the Maple OIT please ensure that all selected PLC memory addresses are valid for your PLC model.

Do not configure the Maple OIT to write to any PLC memory address which should only be written to by the PLC.

On using Bank 8 or Bank 16 formats

When using these formats, each PLC coil (bit) is individually displayed in terms of 1 and 0, with the lowest addressed coil of each 8 coil bank (byte) displayed in the right-most position in that bank. For a Bank 16 format, the lowest address 8 coil bank (byte) is displayed in the left most position.

Therefore, for a Bank 16 format using coils Q0.0 to Q1.7, Q0.0 will be in the ninth coil position from the right and Q1.7 will be in the eighth coil position from the right. Q1.0 will be in the right most display position and Q0.7 will be in the left most display position.

On Using the PLC Clock/Calendar Register (excludes CPU212)

The following addresses apply to the PLC Clock/Calendar Register:

Address 0 - PLC Year, 4-digit BCD, YYYY

Address 1 - PLC Date, 4-digit BCD, HHMM

Address 2 - PLC Clock, 4-digit BCD, MMDD

Since the above information comes from the PLC as 4-digit BCD, that is the recommended format for displaying with the Register Monitor.

OITware-200 Settings

The following table lists the communications settings that must be configured in OITware-200.

Please note:

- the Default column lists OITware-200's default setting; your PLC's default may be different
- the Options column lists OITware-200's options; your PLC may not support every option

| Name | Default | Options | Important Notes |
|-------------------------------------|---------|---|--|
| Baud Rate | 9600 | 19200, 9600, 4800, 2400, 1200, 600, 300 | Must match the PLC port settings. Use the fastest baud rate supported by both. |
| Parity | Even | Even, Odd, None, Mark, Space | Must match the PLC port settings. |
| Data Bits | 8 | 7, 8 | Must match the PLC port settings. |
| Stop Bits | 1 | 1, 2 | Must match the PLC port settings. |
| Status Coils | M0.0 | M0.0 to M30.0 | Must be within the PLC's supported memory range. |
| Address | 2 | 2-31 | Must match address set in PLC. |
| Source Address, Destination Address | N/A | | |
| Password | N/A | | |
| Message Request Register | V512.0 | V0.0 to V5118.0 | Must be within the PLC's supported memory range. |
| Current Message Register (optional) | V514.0 | V0.0 to V5118.0 | Must be within the PLC's supported memory range. |

| Name | Default | Options | Important Notes |
|--|---------|---------------|---|
| Function Key Coils (optional) | M2.0 | M0.0 to M30.0 | Must be within the PLC's supported memory range. |
| Screen Dependent Function Key Coils (optional) | M4.0 | M0.0 to M30.0 | Must be within the PLC's supported memory range. Applies to OITs with Screen Dependent Function Keys. |
| Control Key Coils (optional) | M8.0 | M0.0 to M30.0 | Must be within the PLC's supported memory range. |
| Status LED Coils (optional) | M0.0 | M0.0 to M30.0 | Must be within the PLC's supported memory range. Applies to OITs with Status LEDs. |
| Function Key LED Coils (optional) | M6.0 | M0.0 to M30.0 | Must be within the PLC's supported memory range. Applies to OITs with Function Key LEDs. |

MAPware-100 Settings

The following table lists the communications settings that must be configured in MAPware-100. Please note:

- the Default column lists MAPware-100's default setting; your PLC's default may be different
- the Options column lists MAPware-100's options; your PLC may not support every option

| Name | Default | Options | Important Notes |
|-------------------------------------|---------|---|--|
| Baud Rate | 9600 | 19200, 9600, 4800, 2400, 1200, 600, 300 | Must match the PLC port settings. Use the fastest baud rate supported by both. |
| Parity | Even | Even, Odd, None, Mark, Space | Must match the PLC port settings. |
| Data Bits | 8 | 7, 8 | Must match the PLC port settings. |
| Stop Bits | 1 | 1, 2 | Must match the PLC port settings. |
| Status Coils | M0.0 | M0.0 to M30.0 | Must be within the PLC's support memory range. |
| Address | 2 | 2-31 | Must match the address set in PLC. |
| Source Address, Destination Address | N/A | | |
| Password | N/A | | |
| Message Request Register | V512.0 | V0.0 to V4094.0 | Must be within the PLC's supported memory range. |
| Function Key Coils (optional) | M2.0 | M0.0 to M30.0 | Must be within the PLC's supported memory range. |

PLC Error Messages

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| <p>“OIT Internal Protocol Error ##” An internal error occurred in the OIT. Contact Maple Systems Technical Support.</p> |
| <p>“OIT/PLC Communication Error ###” An error occurred during communication between the OIT and the PLC. Communication errors are most likely due to excessive noise on the communication cable.</p> |
| <p>“No Connection to PLC” The OIT cannot communicate with the PLC. This is most likely due to a broken cable, a broken connector, or a disconnected or loose connector.</p> |
| <p>“Invalid PLC Data Address” A data address outside the memory range of the PLC was entered into the Register Monitor. Recheck the memory ranges available for the CPU and the register monitor settings in OITware.</p> |
| <p>“Invalid PLC Data Type Access” An attempt was made to access a PLC memory location in an invalid fashion. Most likely, this was caused by a write to a read-only object or using the incorrect data length for the data object. Recheck the valid access methods for the memory areas available for the CPU and the register monitor settings in OITware.</p> |
| <p>“Invalid PLC Data Object Access” An attempt was made to access a PLC data object (such as a Counter, Timer, or High Speed Counter) in an invalid fashion. Most likely, this was caused by a write to a read-only object or using the incorrect data length for the data object (e.g.. a byte read of a counter or timer). Recheck the valid access methods for the data objects for the CPU and the register monitor settings in OITware.</p> |
| <p>“PLC Hardware Fault During Data Access” Hardware error in the PLC. Contact Siemens Technical Support if this reoccurs.</p> |
| <p>“Time/Date Not Supported by PLC” Attempt to access the TOD clock on a CPU 212.</p> |
| <p>“Time/Date Values Out of Range” Attempt to initialize the TOD clock to an invalid setting.</p> |